WHAT IS CLAIMED IS:

1. A semiconductor device including a memory cell region and a peripheral circuit region, comprising:

a semiconductor substrate having a major surface;

an insulating film, having an upper surface, being formed on said major surface of said semiconductor substrate to extend from said memory cell region to said peripheral circuit region;

a capacitor lower electrode being formed on said major surface of said semiconductor substrate to upwardly extend beyond said upper surface of said insulating film in said memory cell region; and

a capacitor upper electrode being formed on said capacitor lower electrode through a dielectric film to extend onto said upper surface of said insulating film,

said capacitor lower electrode including a capacitor lower electrode part upwardly extending in opposition to said capacitor upper electrode and having a top surface and a bottom surface,

said upper surface of said insulating film being located between said top surface and said bottom surface of said capacitor lower electrode part.

2. The semiconductor device in accordance with claim

1, wherein

said capacitor lower electrode includes first and second capacitor lower electrodes,

said first and second capacitor lower electrodes are adjacent to each other through a part of said insulating film in said memory cell region, and

said part of said insulating film has a width being smaller than the minimum working size formable by photolithography.

3. The semiconductor device in accordance with claim 1, further comprising a side wall electrode part being formed on a side surface of said capacitor lower electrode located upward beyond said upper surface of said insulating film.

4. The semiconductor device in accordance with claim 1, comprising said dielectric film being formed between at least either a side surface or only a part of said bottom surface of said capacitor lower electrode part and said insulating film.

5. The semiconductor device in accordance with claim 1, further comprising granular crystals on a surface of said capacitor lower electrode.

6. The semiconductor device in accordance with claim 1, further comprising:

a first wiring layer being formed on said major surface of said semiconductor substrate in a region located under said capacitor lower electrode, and

a first interlayer isolation film being formed on said first wiring layer to be in contact with said first wiring layer and said capacitor lower electrode part.

7. The semiconductor device in accordance with claim 1, further comprising:

a first conductive region being formed on said major surface of said semiconductor substrate in a region located under said capacitor lower electrode,

a second interlayer isolation film being formed on said first conductive region and having a first contact hole exposing a surface of said first conductive region,

a second wiring layer being formed on said second interlayer isolation film, and

a connecting conductor film being formed in said first contact hole for electrically connecting said first conductive region with said second wiring layer,

the width of said second wiring layer being smaller than that of said first contact hole.

8. The semiconductor device in accordance with claim 1, further comprising:

a second conductive region being formed on said major surface of said semiconductor substrate in a region located under said capacitor lower electrode,

a third interlayer isolation film being formed on said second conductive region and having a second contact hole exposing a surface of said second conductive region,

a third wiring layer being formed on said third interlayer isolation film,

a wire protection film being formed on said third wiring layer, and

a conductor film being formed in said second contact hole for electrically connecting said second conductive region with said capacitor lower electrode,

said wire protection film being in contact with said capacitor lower electrode or said conductor film.

9. The semiconductor device in accordance with claim 1, comprising:

said capacitor upper electrode being formed to extend toward said peripheral circuit region,

a fourth interlayer isolation film being formed on said capacitor upper electrode and having a third contact hole exposing a surface of said capacitor upper electrode,

and

a peripheral circuit element protection film being formed under said insulating film in a region located under said third contact hole.

10. The semiconductor device in accordance with claim 1, further comprising:

a peripheral circuit insulating film having a peripheral circuit region opening in said peripheral circuit region,

said capacitor upper electrode being formed to extend into said peripheral circuit region opening, and

a fourth interlayer isolation film being formed on said peripheral circuit region opening and having a fourth contact hole exposing a surface of said capacitor upper electrode.

11. The semiconductor device in accordance with claim 1, comprising:

said capacitor upper electrode being formed to extend toward said peripheral circuit region,

a fourth interlayer isolation film being formed on said capacitor upper electrode and having a fifth contact hole exposing a surface of said capacitor upper electrode, and

a peripheral circuit element being formed under said insulating film in said peripheral circuit region,

said fifth contact hole being formed in a region not overlapping with said peripheral circuit element in plane.

12. A semiconductor device including a memory cell region and a peripheral circuit region, comprising:

a semiconductor substrate having a major surface;

an insulating film, having an upper surface, being formed on said major surface of said semiconductor substrate to extend from said memory cell region to said peripheral circuit region;

a capacitor lower electrode, including first and second lower electrodes being adjacent to each other through a part of said insulating film, being formed on said major surface of said semiconductor substrate to extend up to a vertical position substantially identical to that of said upper surface of said insulating film in said memory cell region; and

a capacitor upper electrode being formed on said capacitor lower electrode through a dielectric film to extend onto said upper surface of said insulating film,

said capacitor lower electrode including a capacitor lower electrode part upwardly extending in opposition to said capacitor upper electrode and having a top surface

and a bottom surface,

said part of said insulating film having a width being smaller than the minimum working size formable by photolithography.

13. The semiconductor device in accordance with claim 12, wherein

a side surface of said capacitor lower electrode has a curved plane.

14. The semiconductor device in accordance with claim 12, wherein

said insulating film includes an upper insulating film and a lower insulating film being different in etching rate from each other.

15. The semiconductor device in accordance with claim 12, comprising said dielectric film being formed between at least either a side surface or only a part of said bottom surface of said capacitor lower electrode part and said insulating film.

16. The semiconductor device in accordance with claim 12, further comprising granular crystals on a surface of said capacitor lower electrode.

17. A method of fabricating a semiconductor device including a memory cell region and a peripheral circuit region, comprising steps of:

forming an insulating film having an upper surface on a major surface of a semiconductor substrate to extend from said memory cell region to said peripheral circuit region;

partially removing said insulating film by etching in said memory cell region thereby forming an opening;

forming a capacitor lower electrode in said opening on said major surface of said semiconductor substrate; and

forming a capacitor upper electrode on said capacitor lower electrode through a dielectric film to extend onto said upper surface of said insulating film,

said step of forming said capacitor lower electrode including a step of forming a capacitor lower electrode part upwardly extending in opposition to said capacitor upper electrode and having a top surface and a bottom surface,

said step of forming said insulating film including a step of locating said upper surface of said insulating film between said top surface and said bottom surface of said capacitor lower electrode part.

18. The method of fabricating a semiconductor device

in accordance with claim 17, wherein

said step of forming said insulating film includes steps of:

forming a lower insulating film, and

forming an upper insulating film being different in etching rate from said lower insulating film on said lower insulating film,

said step of locating said upper surface of said insulating film between said top surface and said bottom surface of said capacitor lower electrode part including a step of removing said upper insulating film.

19. The method of fabricating a semiconductor device in accordance with claim 17, wherein

said step of locating said upper surface of said insulating film between said top surface and said bottom surface of said capacitor lower electrode part includes a step of partially removing said insulating film by etching.

20. The method of fabricating a semiconductor device in accordance with claim 17, further comprising steps of:

forming a conductive region on said major surface of said semiconductor substrate in a region located under said capacitor lower electrode,

forming an interlayer isolation film on said

conductive region,

forming a wiring layer on said interlayer isolation film,

forming a wire protection film on said wiring layer, and

removing a part of at least said interlayer insulating film by etching thereby forming a contact hole for electrically connecting said conductive region with said capacitor lower electrode,

said wire protection film being employed as a part of a mask employed for etching in said step of forming said contact hole.

Add A1

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